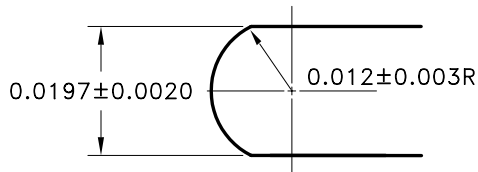
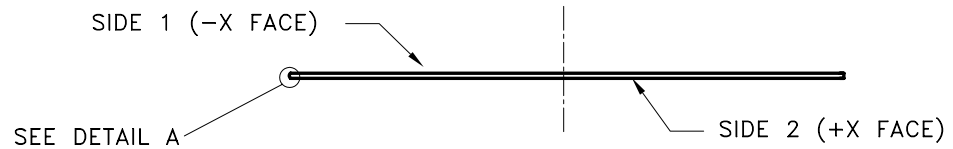
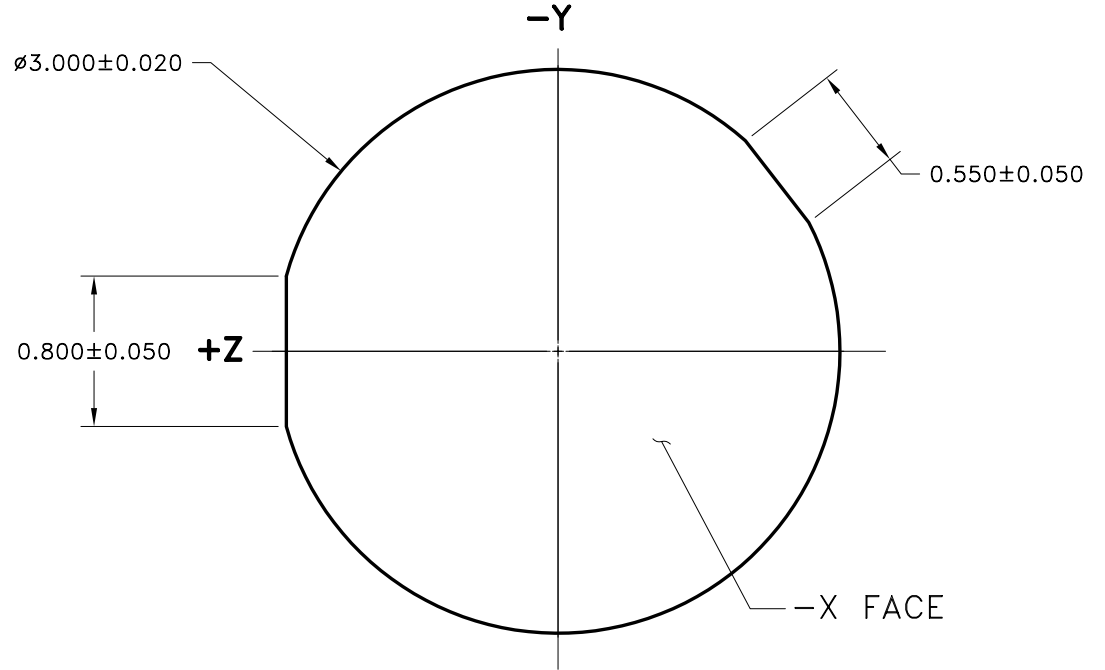


NOTES:


- 1.0 All dimensions are in inches.
- 2.0 ORIENTATIONS
 - 2.1 Wafer surface is NORMAL to the X Axis $\pm 0.5^\circ$.
 - 2.2 Wafer Flat
 - 2.2.1 Primary Flat, Perpendicular to the +Z AXIS $\pm 0.5^\circ$.
 - 2.2.2 Secondary Flat 135° clockwise from the primary flat when viewing the -X polished face.
- 3.0 EDGE
 - 3.1 All edges rounded with a $R=0.012\pm 0.003$ radius.
 - 3.2 No chips greater than 0.020 inches penetration and 0.039 inches in length.
- 4.0 SURFACES
 - 4.1 SIDE 1 <-X> face
Polished 10-5 scratch-dig with 1mm edge exclusion. No pits or scratches visible with reflected light and unaided eye.
 - 4.2 SIDE 2 <+X> face
Polished 20-10 scratch-dig with 1mm edge exclusion. No pits or scratches visible with reflected light and unaided eye.
- 5.0 FLATNESS
 - 5.1 WARP <20um.
 - 5.2 T.T.V <10um.

REVISIONS					
ZONE	REV	DESCRIPTION	ECO NO.	APPD.	DATE
ALL	B	UPDATE PER EO	18530	KH Chan	08/30/10



DETAIL A
SCALE: 25X

Document
09/03/10
Control

FINISH: SEE NOTES		CONTRACT NUMBER		 Crystal Technology, Inc. A Group Company of TDK-EPC Corporation
MATERIAL: LN		DR. Geri Scholz	08/30/10	
SPEC. NO.		CHK.		TITLE: LN WAFER, 3.00 ϕ X0.0197 (X) POL/POL 0.800" +Z FLT 0.550" SECONDARY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		APPD.		
TOLERANCES		APPD.		SIZE: A
INCHES	MILLIMETERS	Wafer Code: LNA--X:076.020DN		DWG. NO. 99-00629-01
.XX \pm .01	X.XX \pm 0.25	CUSTOMER APPROVAL:		REV. B
.XXX \pm .005	X.XXX \pm 0.125			
.XXX \pm .0020				
ANG \pm .5°				
		DO NOT SCALE DRAWING		SCALE: N/A
				SH. 1 OF 1

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