

Notes:

1.0 Orientations

- 1.1 Wafer surface is normal to X axis $\pm 0.5^\circ$
- 1.2 Flats
 - 1.2.1 Primary flat is normal to $\langle +Z \rangle \pm 0.5^\circ$.
 - 1.2.2 Secondary flat is $135^\circ \pm 1^\circ$ clockwise from the primary flat when viewing the $-X$ face.

3.0 Edge

- 3.1 All edges rounded with $R0.27 \pm 0.08\text{mm}$.
- 3.2 No chips greater than 0.5mm in penetration and 1.0mm in length.

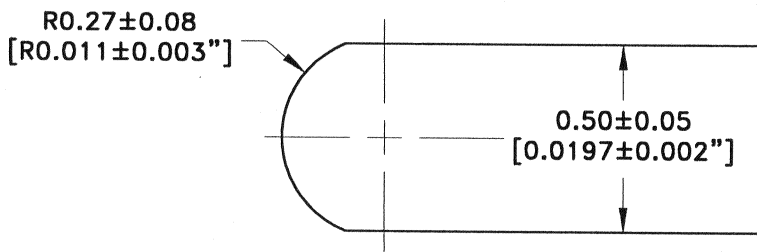
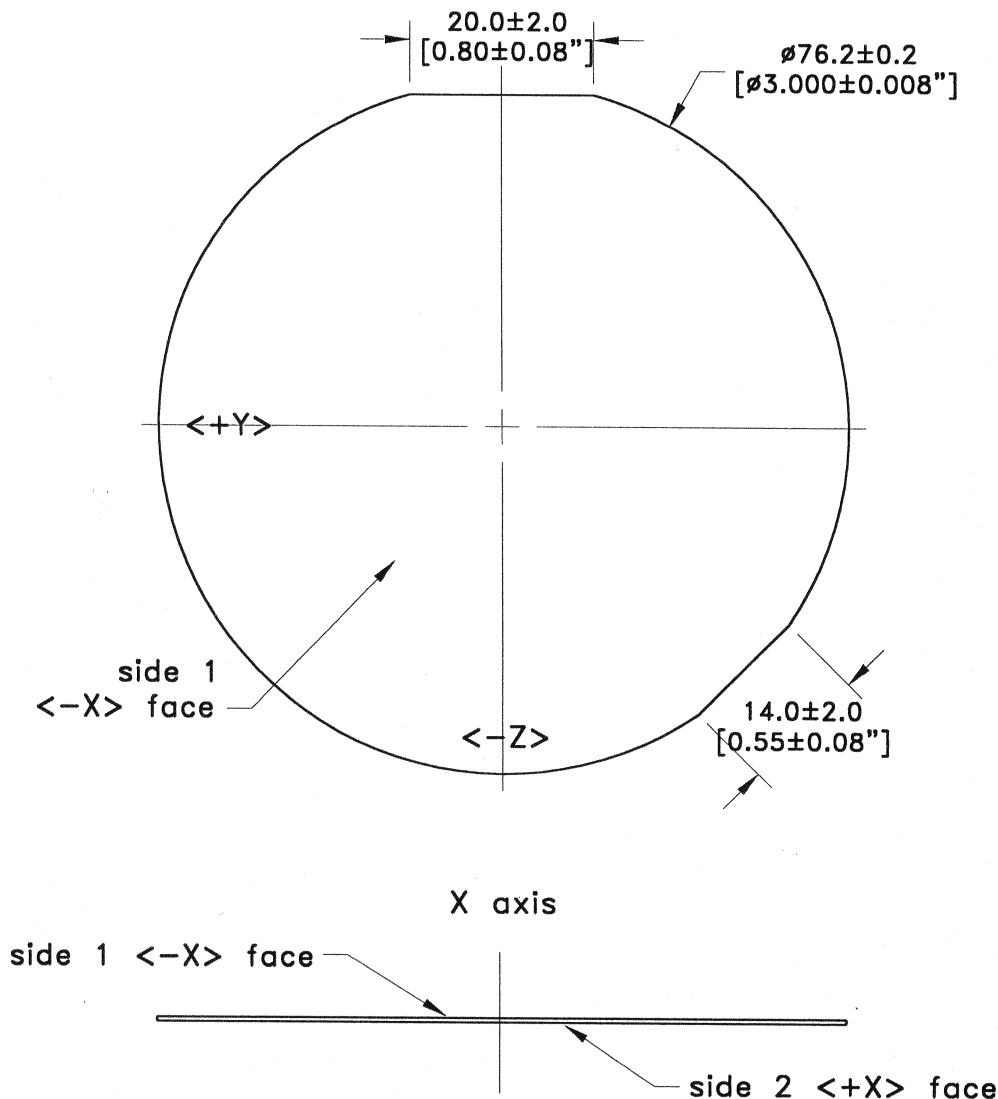
4.0 Surfaces

- 4.1 Side 1 $\langle -X \rangle$ face
Polished 10-5 scratch-dig with 1mm edge exclusion.
No pits or scratches visible with reflected light and unaided eye.
- 4.2 Side 2 $\langle +X \rangle$ face
Ground, R_a 0.50-0.70 μm .

DOCUMENT

AUG 25 2003

CONTROL



Wafer Edge Detail, 50:1

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Material: Lithium Niobate		DR. Igordon	08-25-03	Crystal Technology, Inc. An EPCOS Company
Unless otherwise specified, dimensions in mm		CHK.		
Tolerances		APPD.		Title: LNIO 76.2 ϕ x 0.5mm, -X Po/Gr, +Z FLT Wafer Code: LNA--X:076.050CN
Inches	Millimeters	Customer Approval:		
X \pm 0.1	X \pm 0.5			Size: A
XX \pm 0.01	X \pm 0.25			Dwg. No: 97-01183-01
XXX \pm 0.005	.XX \pm 0.1			Rev: D
.XXXX \pm 0.0020	.XXX \pm 0.05			Scale: 1.2:1
Angles \pm 0.5°		DO NOT SCALE DRAWING		Sheet 1 of 1